Remarks/Arguments

Reconsideration of this application is requested.

Claim Status

Claims 11-22 are pending in this application. Claims 1-10 are canceled.

Drawings

The drawings are objected to under 37 CFR 1.83(a) for not showing the step of comparing the detected current with the reference current. While applicant believes that this step is already adequately described in the specification and drawings, applicant submits herewith a new drawing sheet including a new Figure 10. New Figure 10 merely conforms the drawings to the specification, and tracks the description from page 5, line 30 to page 6, line 5. This portion of the specification has been amended to include appropriate reference to the new Fig. 10. A description of Fig. 10 is also added to the "Brief Description of the Drawings" section on page 4.

Figures 1, 3 and 5 are also objected to for failure to label boxes. In particular, the Action asserts that boxes 12-1 through 12-N of Figures 1 and 3 should be labeled "D/A Conv.", that box 52 of Figure 3 should be labeled "Signal Control Section", and that box 72 of Figure 5 should be labeled "Input Latch Circuit". In this regards, applicant assumes that the Action intended to refer to Figure 4 for box 52. Replacement sheets 1 and 3-5 are enclosed, including Figures 1 and 3-5, incorporating the revisions suggested by the Examiner. In addition, in Figures 1 and 3, box 14 is labeled "Voltage Follower Group" and box 26 is labeled "Switching Element Group".

No new matter is added by these amendments to the drawings. With respect to replacement sheets 1 and 3-5, applicant notes that these correspond to the formal drawings submitted in parent application 09/880,712 (U.S. patent 6,633,167). New Figure 10 merely conforms the drawings to the specification, and tracks the description from page 5, line 30 to page 6, line 5.

Double Patenting – Terminal Disclaimer

Claims 11-22 are pending in this application and are rejected under the judicially created doctrine of obviousness-type double patenting as being obvious over claims 1-10 of U.S. patent 6,633,167. Enclosed to overcome this rejection is a terminal disclaimer.

Claim Rejections – 35 USC 102 and 103

Claims 11-16, 21 and 22 are rejected under 35 USC 102(b) as anticipated by Ooishi (USPN 6,205,071). Applicant traverses these rejections and asserts that Ooishi does not disclose each and every limitation as recited in claims 11-16, 21 and 22. In particular, Ooishi does not teach or suggest, "short-circuiting each of the plurality of output lines upon examination" and "comparing a current value detected on the short-circuited lines and a specified current value to thereby determine whether the signal supply apparatus is good or bad," as required by independent Claim 11. Identical or extremely similar limitations are present in claims 12-16, 21 and 22.

Ooishi is directed to a semiconductor memory device having a shorting circuit 450 as shown in FIGS. 19-20. Shorting circuit 450 is provided at the sense amplifier band to selectively short-circuit sense amplifier drive signal lines SE and SE1 and bit line isolation control signal lines BLIL and BLIR. *See Ooishi, column 22, lines 1-4.* The purpose of shorting circuit 450 is to reduce the voltage level of a selected bit line isolation control signal. *See Ooishi, column 22, lines 13-15.* Shorting circuit 450 includes switch circuits 456, 457, 458 that set the BLIL, SE, SE1, and BLIR signals to the same voltage level when conducting. *See Ooishi, column 22, line 49 to column 23, line 2.* Ooishi is not concerned with examining the signal supply circuits, such as circuit 420 in FIG. 8 for generating signal SE and circuit 440 in FIG. 16 for generating signal SE1, to determine whether these signal supply circuits are good or bad. Instead, in Ooishi, switch circuits 456, 457, 458 are short-circuited to equalize the signals BLIL, SE, and SE1 to the same voltage level. *See Ooishi, column 24, lines 4-5.*

In contrast, claims 11-16, 21 and 22 require short-circuiting output lines upon examination and comparing a current value detected on the short-circuited lines and a specified current value to thereby determine whether the signal supply apparatus is good or bad. As described above, this is not disclosed or taught by Ooishi. Since Ooishi does not teach or disclose each and every limitation of claims 11-16, 21 and 22, it cannot anticipate those claims.

Claims 19 and 20 are rejected under 35 USC 103(a) as obvious over Ooishi. Applicant traverses these rejections and asserts that claims 19 and 20 distinguish over Ooishi for the same reasons as set forth above with respect to claims 11-16, 21 and 22.

Claims 17-18

There being no rejections of claims 17 and 18 beyond the double patenting rejection, in view of the enclosed terminal disclaimer, applicant submits that claims 17 and 18 are allowable.

Conclusion

This application is now believed to be in condition for allowance. The Examiner is invited to contact the undersigned should any issues remain after entry of this amendment. Any fees due with this response may be charged to our Deposit Account No. 50-1314.

Respectfully submitted,
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Amendments to the Drawings

The attached four replacement sheets include changes to Figures 1 and 3-5. These sheets, which include Figures 1 and 3-5, replace the original drawing sheets including Figures 1 and 3-5. In Figures 1 and 3, boxes 12-1 through 12-N are labeled "D/A Conv.", box 14 is labeled "Voltage Follower Group" and box 26 is labeled "Switching Element Group". In Figure 4, box 52 is labeled "Signal Control Section". In Figure 5, box 72 is labeled "Input Latch Circuit".

The attached new sheet includes a new Figure 10.